iW-PCIe to UART Bridge

Introduction

The iW-PCIe to UART Bridge consists of a single UART controller & a Xilinx endpoint core for PCIe with PHY interface. The PCIe to UART bridge is a 32 bit PCI express interface that fits into a single Spartan3 FPGA

Features

PCIe Interface :

- 32 bit PCIe interface with Xilinx endpoint core for PCIe with external PHY hardware.
- The Xilinx endpoint core for PCIe follows PCI express base specification v1.1 layering model
- Endpoint core implements the physical layer, datalink layer, transaction layer & configuration management layer
- Six individually programmable BAR's & expansion ROM BAR
- MSI & INTX emulation.
- Removal of corrupt packets for error detection and recovery
- Compatible with PCI/PCI Express power management functions
- Used in conjunction with NXP PX1011A PCI Express standalone PHY to achieve high transceiver capability
- 2.5 Gbps line speed, Automatic clock and data recovery, 8b/10b encode and decode
- Maximum transaction payload of up to 512 bytes

UART Interface :

- RS-232-C protocol support
- Asynchronous communication only
- Serial interrupt support
- Clock rates of baud rate x 16 or baud rate x 64
- Character length of 7 or 8 bits
- 1 or 2 Stop bits
- Break transmission
- Automatic break detection
- Full duplex double buffer system
- Parity addition/checking
- Error detection for parity, overrun and framing

Description

The PCIe Bridge has an endpoint PIPE v1.7 (PHY Interface) for PCIe 1 lane core from Xilinx, Programmed I/O module &UART controller. The endpoint core from Xilinx implements the physical layer (PHY interface), data link layer, transaction layer & configuration management layer of PCIe base specification v1.1 layering model. A external PCIe PHY device is needed in the PHY Interface side to complete the 1 lane PCIe link.The PIO design interfaces with the endpoint for PCIe core's transaction interface & responds with read/write transaction for memory or IO transaction from the endpoint core.

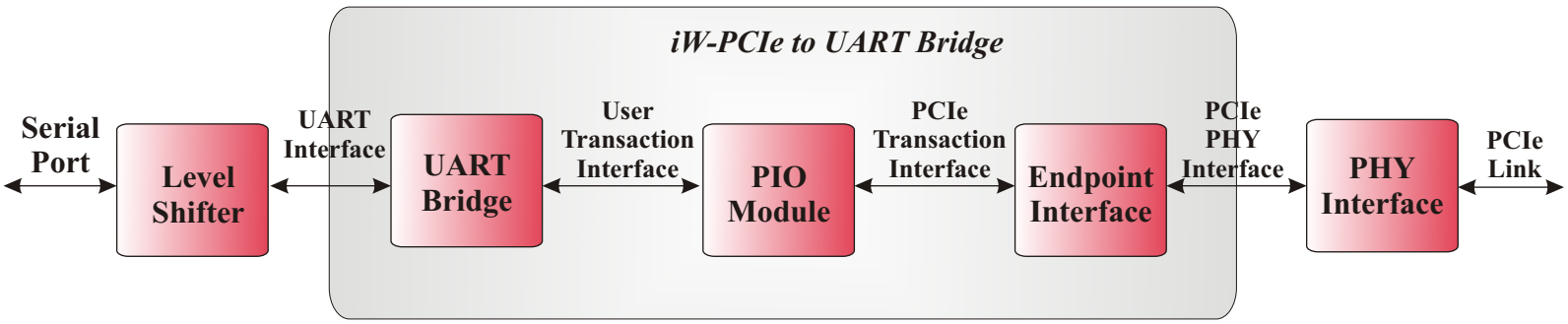
The UART controller is implemented in user interface side of the PIO design. The Serial Controller Unit is an UART based on with support for asynchronous communication only. The processor can access the unit through I/O read and write commands. The SCU converts parallel data from the host processor to serial data and transmit it and convert the serial received data into parallel data for the host processor to read. The start bit, parity bit and the stop bits are automatically added in the transmit direction and is stripped in the receive direction. PCIe bridge supports the 32 bit data transfer between the host CPU & the modem in UART bridge side in conjunction with the level shifters for DB9 connection.

Example Application

The below diagram shows the example application for the PCIe to UART bridge, which requires a additional PHY device & level shifters to connect a computer modem to another host CPU through PCIe link.

The PCIe to UART bridge requires a standalone PHY hardware to form a complete PCIe link. The PHY handles the low level PCIe protocols & signaling. The UART requires a additional level shifters to connect the DB9 connector, with this setup it is possible to communicate between the host CPU & the computer modem using UART bridge through 32 bit PCIe interface.

Figure-1 : PCIe to UART bridge Block Diagram & Example Application



Device Utilization Summary

IP	Xilinx Device	Fmax (MHz)	Slices	4 input LUTs	IOB	GCLK	BRAM	DCM	Power (mW)	Design Tool
PCIe to UART Bridge	XC3S700A	107	4,919 (83%)	6,972 (59%)	37 (11%)	7 (29%)	8 (40%)	2 (25%)	66	9.2.04i